In the Autumn of 1992 I designed a processor that would use only TTL-logic chips. I didn't actually build it, which would have required hundreds (probably thousands) of chips, and days containing significantly more than the standard 24 hours provided. This page contains scans of my (incomplete) design notes.

This processor is particularly unusual in that it is an asynchronous processor. In a normal processor, every activity is coordinated by a clock signal. An asychronous processor has no clock signal, every part of the circuit does its processing as fast as possible and signals subsequent circuits when it is complete.

The advantage of this approach is that every part of the circuit can run at optimum speed. In a "normal" synchronous processor, the speed is often limited by the speed of the slowest part.

Asynchronous devices also consume less power. In conventional processors, much of the power is eaten up by the clock generator: a powerful clock signal is required because it must propagate as quickly as possible to all areas of the chip. Asynchronous processors generate much less electromagnetic interference (EMI) because activity is not coordinated to occur at the same precise times, which causes power spikes. The lower power consumption and EMI were obviously not even a consideration for my TTL monster processor, and in fact I didn't even think about them.

I had never heard of asynchronous processing and thought it a very innovative idea. Later (much later) I learnt that asynchronous processors were already under development elsewhere (often you think you invented something and later find someone else has already had the same idea). The University of Manchester AMULET group was started in 1990 and has designed a number of ARM-compatible asynchronous processors.

I thought that being asynchronous would give me high performance. My design notes are incomplete and surely would have required considerable further development before being workable. But I do believe the basic principles could have led to a functioning TTL asynchronous processor. The features of this processor are as follows:

o 40-bit word size.
o 20-bit address space (5 MByte), includes DRAM controller.
o 20-bit instructions, with a few 40-bit. 2 20-bit instructions fit in one word.
o RISC Z80-like instruction set
o 10 general purpose 40-bit registers
o Floating point format: 1 sign bit, 8 exponent bits, 39 fractional bits
o Includes integer and floating point addition, subtraction and multiplication units
o Controlled, including all I/O by a Z80-based host computer .

There are 59 scanned pages, each has an accompanying textual description of what I was thinking of, when I wrote that page.

CLICK HERE to DOWNLOAD the whole document (5.2MBytes)