

CPCNG notes: CPC compatibility

Written by Hans Summers

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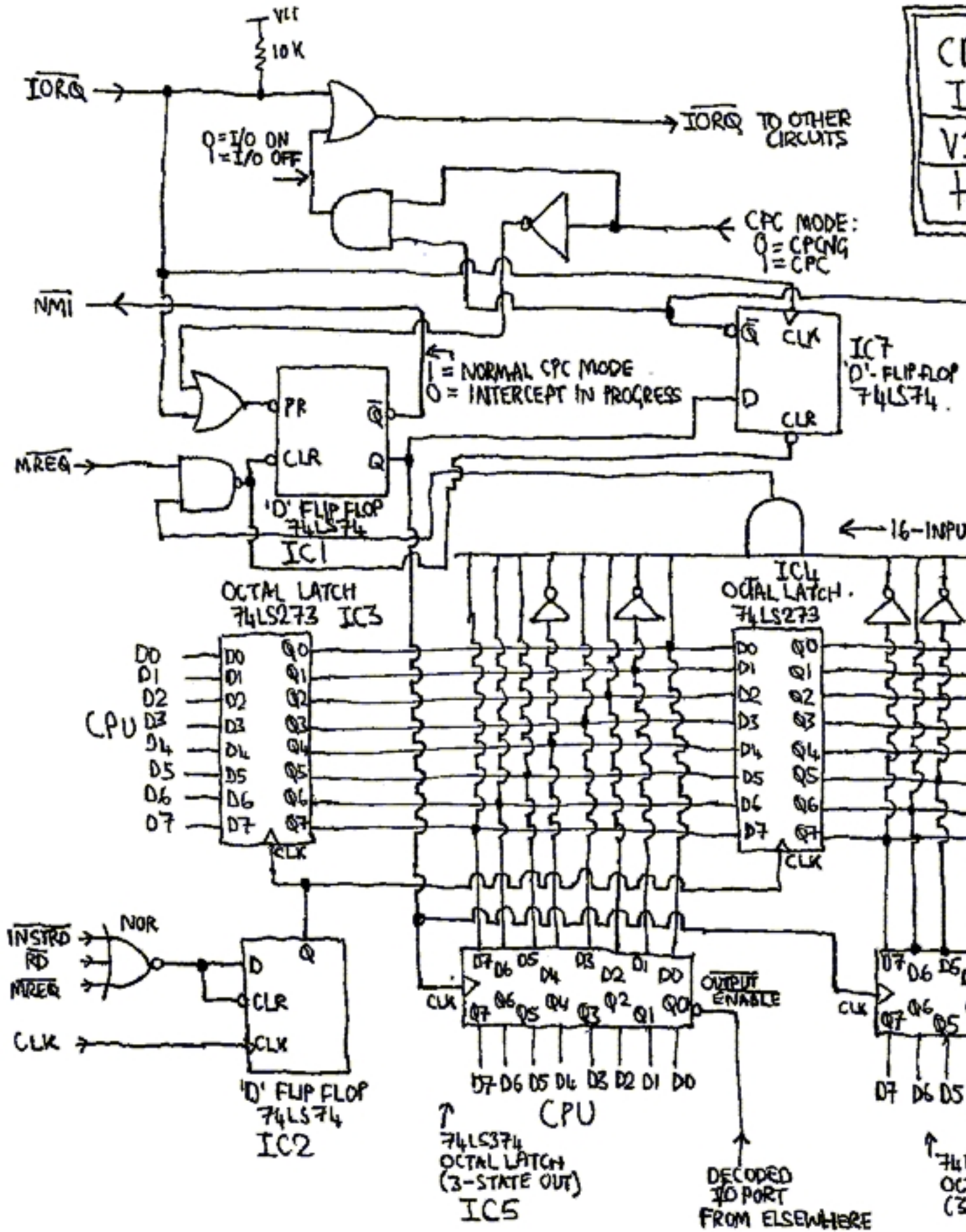
This is a draft design for the CPC-compatibility circuit. This logic will reside in the FPGA, and will equip the CPCNG with a CPC-compatibility mode in which almost all old CPC software will run. Exceptions will be anything which makes use of precise timing, since the eZ80 runs at a totally different pace to the old Z80, the video memory arbitration is organised differently in the CPCNG, and there is an extra overhead associated with translation and emulation of CPC I/O.

Refer to the below diagram of the CPC-compatibility circuit. If we use schematic entry for the FPGA we can enter this circuit for the I/O intercept trick. I have marked the main chips in this design with equivalent TTL 74LS-series part numbers, just so that their functionality is well defined (in reality 74LS logic would be too slow to be able to build this circuit for real).

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