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Introduction

This was my first frequency counter project. It includes ... LM324 quad op-amp ... a variety of different ... {gallery} ... features ...

Specifications

- Pulse counter (0 to 80,000,000)
- Frequency counter
- Pulse width measurement
- Visible TTL logic probe, LED is Red for 0, Green for 1 and Yellow for don't care (in between)
- Audible TTL logic probe, a low sound for 0, high sound for 1. Quickly changing logic levels cause a sort of warble!
- Edge-triggered timer (selectable positive or negative edge)
- Push button start/stop timer
- 5 timing resolutions: 1 uS, 1 mS, 10 mS, 100 mS, 1 s
- 4 frequency measurement ranges 1Hz, 10 Hz, 100 Hz, 1 KHz taking 0.5, 5, 50 and 500 readings per second respectively

As can be seen, quite a comprehensive piece of test equipment! The only thing I never did finish, which I should have, was a pre-amplifier. As it was, the signals fed in had to be TTL level, which was useful when measuring frequencies and testing digital circuits, but would have been a problem with analogue circuits.

The Circuit Diagram

CLICK HERE to download the 4 pages of the circuit diagram (schematic) in Adobe Acrobat .pdf document format (size 403K). The pages are:

Page 1: Logic tester
Page 2: Timing logic & voltage regulator
Page 3: Timing chain, counters, display decoding logic
Page 4: Display drivers and 7-segment LED displays

I will now attempt to explain the theory behind the operation of this circuit. At all times remember that I built this project aged 17 on a budget of practically zero. Therefore almost all the components are from old dismantled equipment, which means that I made use of what I had rather than designed the circuit in the most efficient, effective or economical way. In certain places I constructed AND, OR etc gates from combinations of resistors, diodes and transistors to avoid having to use a specific TTL part. All such transistors are any suitable small signal

transistor, I used mostly things like 2N2222, BC108 etc.

First an explanation of the switches and buttons' functions:

S1 +/- Edge: Selects the polarity of the input. For the timer and pulse-width measurement modes, this switch selects whether the timer will start/stop on the positive or negative-going edge of the input pulse. In frequency counter mode, the setting isn't really relevant.
S2 Mode: The main mode switch, switches the whole circuit between the frequency counter mode and the timer/pulse width mode.
S3 Range: In frequency mode, selects the resolution of the counter from 1Hz, 10Hz, 100Hz and 1KHz, taking 0.5, 5, 50 and 500 readings per second respectively. In Timer mode, selects the resolution of the timing from 1uS, 1mS, 0.01s, 0.1s and 1s.
S4 Pulse width/Start-stop: Only relevant in the Timer modes. It selects pulse width measurement (i.e. counting occurs while the incoming pulse is high) or start/stop timer (one pulse is required to start the timer, another to stop it).
S5 Logic probe: Switches the logic probe between OFF, ON (LED only) and ON (LED and loudspeaker).
S6 Power: Main power switch for the whole circuit
S7 Hold button: Used to freeze the display. In timer mode, it can be used as a Stop button for manual timing.
S8 Reset button: Used to reset the counters in timer mode.

I'll start with page 1 which is the simplest part of the circuit. This is an audible logic probe. The 10mm tricolour LED on the front panel in fact internally contains a red and a green LED. Two 100K multiturn potentiometers are adjusted to exactly the TTL transition voltage levels (max 0.8V for a zero, min 2.0V for a one). 2 parts of a LM324 quad op-amp are used as a comparator to control the LED's such that when the input voltage is greater than 2.0V (logic "1") only the green LED is lit, when less than 0.8V (logic "0") only the red LED is lit, and when between 0.8 and 2.0V both LED's are lit giving a yellow colour. This gives an immediate visual indication of the incoming logic level. The other two op-amps switch two different capacitors into the frequency-determining circuit of a free-running
555
astable multivibrator. The output of this drives a tiny loudspeaker, whose pitch is high for a "1" and low for a "0". When a pulsing input is applied the LED will show various shades of yellow and orange, and the loudspeaker warbles. This is also a very useful diagnostic indication when you are used to listening to it, to determine if a signal is as you expect it. Switch S5 switches the logic tester On/Off and has three positions which are (from top to bottom): OFF, ON (LED only) and ON (LED and loudspeaker).

Next the timer chain on page 3 of the circuit diagram. This consists of a 4MHz crystal oscillator, first divided by 3 in IC27 to get 1MHz, then further divided by 1000 in IC19 to give 1KHz. Three divide-by-10 counters (IC21, IC22, IC23) give outputs at 100Hz, 10Hz and 1Hz. The range switch S3 selects one of these signals (1Hz, 10Hz, 100Hz, 1KHz or 1MHz) as the "gate time" signal which is sent to the complicated timing logic on page 2.

In the timer mode, this signal is directly counted by the 74LS390 decade counters on page 3.

The period of counting is determined by the input signal. S1 decides whether to act on the positive or negative edge of the incoming signal using XOR gate IC29. S4 selects pulse-width mode, in which the "gate time" frequency is counted for the duration of the incoming signal's high (or low, see S1) period; or start/stop mode, in which one incoming pulse starts the timer and the next pulse stops it. In the latter case IC27a (divide-by-2) counter provides the count enable. In Frequency counter mode, IC27a is used to enable counting, clocked by the "gate time" signal, while counting is done on the actual input frequency to measure. The green "Gate" LED flashes in time with the input pulse in timer mode, or once per measurement in the frequency counter mode (i.e. with the "gate time"). There is also an "infinite" setting (the 6'th setting on the range selector switch S3) in which the incoming frequency is just counted indefinitely (at least, until it reaches 80,000,000).

The circuit around OR-gate IC33c (74LS32) and the 2 transistors below it is effectively a discrete-component implementation of a set/reset latch. Pressing the "Hold" button (S7) causes the output to be a "1" and remain there (due to the diode from the output of IC33c to its input). Pressing the "Reset" button (S8) shorts the OR-gate input to ground which resets the circuit. The second transistor provides an nverted output. The "Hold LED" signal is sent to the red "Hold" LED on page 3.

To the right of the Hold/Reset circuit is some logic to control the resetting of the main counters and latching of their outputs (see IC90, IC31a, IC31b, IC33d, IC31c, IC29c, IC14b, IC29b). In frequency counter mode, there are alternate periods of counting and resting. For example in the 1Hz resolution mode, the counters are clocked by the input frequency for 1 second, then there is a 1 second rest. To maintain a constant display, latches are inserted between the main counters and the display drivers (IC9, 10, 11, 12 on page 3). Latching must occur during the resting period, followed by a resetting of the main counters ready for the next measurement (counting) period. This part of the circuit accomplishes this function. It is clocked by the 1MHz signal from the crystal oscillator divider chain on page 3. IC20 (74LS90) counts from 0 to 4 and then stops and waits on the count of 4 (via the NAND gates IC31a and IC31b at the bottom). The count of 2 is decoded by IC29c (XOR gate used as an invertor) and IC31c (74LS00
NAND gate), and this signal indirectly drives the latches. However, the latch signal is also set during the Timer mode, and when "infinite" count mode is selected, so that in these modes the latches pass through the count without latching it, and the display shows directly the contents of the main counters.

At the top of page 2 comes a curious circuit surrounding IC20, IC29a, IC33b, IC33a, IC14c. The purpose of this circuit is to addionally gate the main counters. It is capable of preventing counting by applying a logic "1" to IC33 pin 2 (the OR-gate). Pin 1 of IC33 comes from the input frequency in frequency counter mode, or in timer mode the timer "gate time" signal (1Hz to 1MHz depending on resolution). In frequency counter mode, S2d (top right of page 2) is open, which means the collector of the adjacent transistor is low voltage (via the 1K resistor to GND). This ensures that whatever the input at the base of the transistor, the input to pin 1 of the 74LS 04
inverter IC28a is always "0", which means that IC20 is non-functional during the frequency counter mode. In the timer mode however IC20 is activated (by applying VCC to the collector of

the transistor via a 560-ohm resistor). IC20 is clocked via the inverter by the output of IC14c (top left of page 2), which is clocked by the timer start/stop signal. The effect of this is for IC20 to allow exactly one counting period, before its Q output (pin 12) becomes "1", which feeds through to IC14 pin 9 and prevents any further counting by the main counters via IC33b pin 4 (OR-gate). It also drives the "Hold" LED. The other input to IC33b (pin 5) is the overflow signal from the main counters, which goes to "1" when the count reaches 80,000,000 and this also suspends further counting. Therefore the whole purpose of this mysterious part of the circuit at the top of page 2 may be summarised as: in Frequency counter mode, do nothing; in Timer mode, time exactly one pulse width (or start/stop cycle) then lock the count (and light "Hold" LED) until reset. This is important as otherwise it would be impossible to view the results of the timing (e.g. short pulse width) since it would be quickly overwritten by the next incoming pulse.

At the bottom of page 2 is the power supply circuit, which is just a conventional voltage regulator using a simple 5V 7805 voltage regulator (IC35) mounted on a small heatsink bolted to the inside of the back of the aluminimum case.

On to page 3 and a much simpler circuit to understand! The main counting chain is made up of four 74LS390 dual BCD counter chips (IC13, 15, 16, 17), for 8 decimal digits of counting. The Q3 output of the final counter (IC17 pin 7) is used as an overflow signal to prevent further counting (see page 2) and light the "Hold" LED which in this case would signal the overflow condition. This occurs at a count of 80,000,000. I'm not sure if the counter is capable of measuring frequencies in excess of 80 MHz (I think it unlikely given the speed specifications of the TTL logic chips used), however you can certainly exceed a count of 80,000,000 easily in the Timer and "infinite" counting modes.

Following the counter chain are four 74100 dual-4-bit latches. These chips latch the data at their input while their "Enable" input is "1" and lock the current values when it goes to "0". These latches are essential to maintain a steady count in the Frequency counter mode during the counting periods (otherwise this frequency counter would be really ugly). The 74100 latches are in a large (0.6 inch width) 24-pin DIL package and totally obsolete. The 74100 is one of the few devices in the original TTL family which didn't make it into the later 74LS-series and 74HC-series etc. families. It was in fact superseded by devices like the 74LS373 which performed a similar function but fit a smaller (0.3 inch width) 20-pin DIL package. I can't even find a datasheet for the 74100, only a basic pinout (see my datsheets page). My only reason for using the 74100 was that I happened to have some available on old computer boards.

The 7-segment display drivers **should** have been straightforward. I used eight 74LS48 drivers, one for each digit. But to my dismay I discovered that the 74LS48

's I had are for driving common cathode 7-segment LED's but the LED's I happened to have were all common anode which should be driven by the
74LS47
chip, of which I had none. Had I used
74LS47
's I would have driven the LED's directly via 220-ohm current limiting resistors, and much of the circuit shown on page 4 would have been unnecessary. Recall my low budget and use of old parts. Due to these factors I had to make do with the mismatching display/display drivers, and the only way to do this was by inverting the
74LS48
outputs. That would have required 56 transistors, one for every segment. Instead I chose to multiplex the display, which meant I only had to use 7 inverting transistors (for one digit) but then I had to use an additional 8 transistors for switching on the appropriate digit, 56 diodes to OR-together the
74LS48
outputs, and some TTL IC's to blank the non-displayed 7 digits and switch on the 8'th's transistor. After all that it probably would have been easier to use 56 inverting transistors, but I probably didn't realise that until I was half way through.

The mechanics of the multiplexing are as follows: IC26 is a 555 timer circuit running as an astable multivibrator at a measured frequency of some 1208 Hz (meaning the display is refreshed 151 times a second). This drives a 3-bit counter IC32b (
74LS93
), which is decoded by a
74LS138
3-8 line decoder. The outputs of this decoder switch on one of the digits, and at the same time via inverters in IC30 and IC28c/d drive the "ripple blanking" inputs of the
74LS48
's, to blank the other 7 digits. Therefore only 1 digit's worth of 7-segments appear at the 7 segment-inverting transistors. The RBO inputs are actually OR'ed with the previous digit's RBI (see
74LS48 datasheet
for more details), so that leading zeroes on the display are blanked. The "LT" (lamp test) input of the
74LS48
's are briefly taken low by a 470uF capacitor on switch on, so that 88888888 is displayed for a short time after switch on.

Construction of this project used my preferred method of tidy point-to-point wiring on plain un-coppered matrix board. Ribbon cable is used for connections between the front panel and the board. The power supply regulator, fuse and miniature speaker are on inside the back of the alumninium box. Four screws at the corners of the board fix it to the almunium box, via "spacers" made from plastic tubing. On the front panel there is a power input socket, a 3.5mm jack-plug socket for the input signal, and parallel black/red probe sockets also for the signal input.

There is currently no input amplifier in this project, so all input signals must be at TTL compatible levels. This has mostly suited me for my usage of the frequency counter and logic probe for debugging other projects, but ideally a suitable input amplifier should be built to protect the input chips and also to permit measurement of small signals.

Photographs

{gallery}counter/1{/gallery}**Front View of the Frequency counter:**

On-off switch is at the top left, to the right of that the TTL logic level indicator light, below that the 6-settin

{gallery}counter/2{/gallery}**The inside view!**

The circuit actually a lot neater than it looks in this picture. The proliferation of ribbon cables connecting